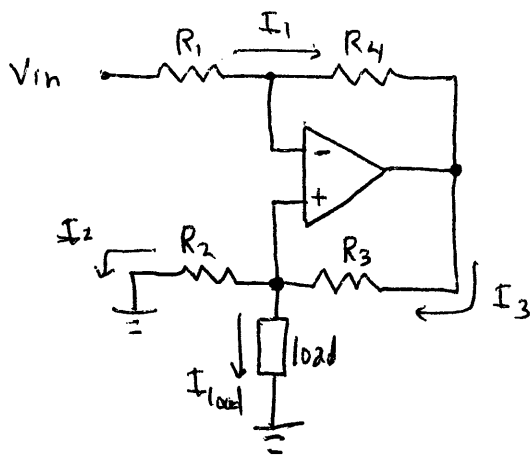


4.2 The Howland Current Source.



Since the op-amp keeps its inputs at the same potential, the voltage across R_4 equals the voltage across R_3

$$-I_3 R_3 = I_1 R_4 \quad (1)$$

↑ to be consistent with directions shown on diagram

Since no current flows into or out of the op-amp inputs (and charge is conserved)

$$I_3 = I_2 + I_{load} \quad (2)$$

Putting (2) into (1) $\Rightarrow I_2 R_3 + I_{load} R_3 = -I_1 R_4$

or... $I_{load} = -I_1 \left(\frac{R_4}{R_3} \right) - I_2$

Now $I_2 = \frac{V_+}{R_2} = \frac{V_-}{R_2}$ since $V_+ = V_-$

and... $V_- = V_{in} - I_1 R_1$, so...

$$I_{load} = -I_1 \left(\frac{R_4}{R_3} \right) - \frac{V_{in}}{R_2} + I_1 \frac{R_1}{R_2}$$

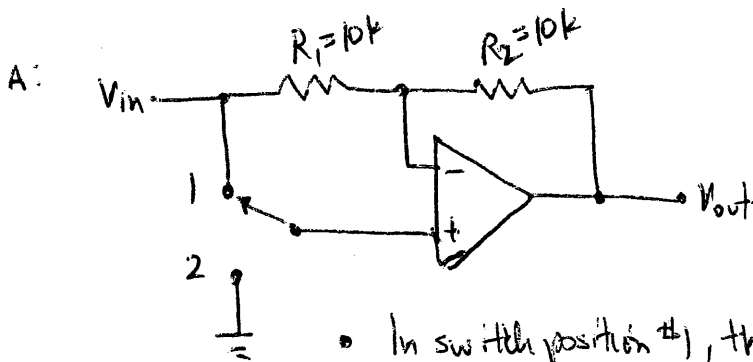
or... $I_{load} = -\frac{V_{in}}{R_2} + I_1 \left[\frac{R_1}{R_2} - \frac{R_4}{R_3} \right]$
 set this to zero...

choosing $\frac{R_1}{R_2} = \frac{R_4}{R_3}$ or $\frac{R_3}{R_2} = \frac{R_4}{R_1}$, then

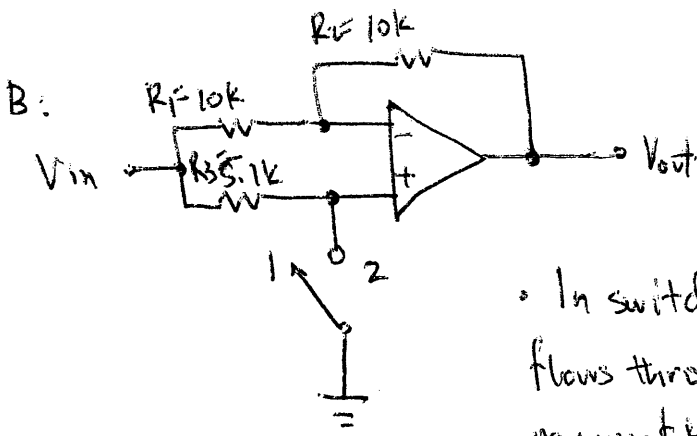
$$I_{load} = -\frac{V_{in}}{R_2}$$

as indicated on p. 182.

4.3 Analyze the "optional inverter" circuits of Fig. 4.14.



- In switch position #1, there is no voltage across the 1st resistor (since $V_+ = V_-$), so no current flows through it. Therefore no current flows through the second resistor either and $V_{out} = V_- = V_+ = V_{in} \Rightarrow$ unity gain follower.
- In switch position #2, we have an inverting amplifier (see Fig. 4.4) with gain $= -\frac{R_2}{R_1} = -1$.



- In switch position #1, no current flows through R_3 (5.1k Ω) since no current flows into an op-amp input.

Therefore $V_+ = V_{in} = V_-$

No voltage appears across R_1 , so no current flows in R_1 or $R_2 \dots V_{out} = V_- = V_+ = V_{in} \Rightarrow$ unity gain follower.

- In switch position #2, $V_+ = 0$, so we have our ordinary inverting amplifier -- (V_- is a virtual ground) with gain $= -\frac{R_2}{R_1} = -1$
 Note that some current flows through R_3 (5.1k Ω) to ground so the input resistance is the parallel combination of R_1 and R_3 .

Ch. 4 Additional Exercise #2: Design a capacitively coupled, non-inverting audio amplifier using an op-amp with gain = 20 dB, $Z_{in} = 10k$, and the -3dB point at 20 Hz

See fig. 4.6 on p. 179

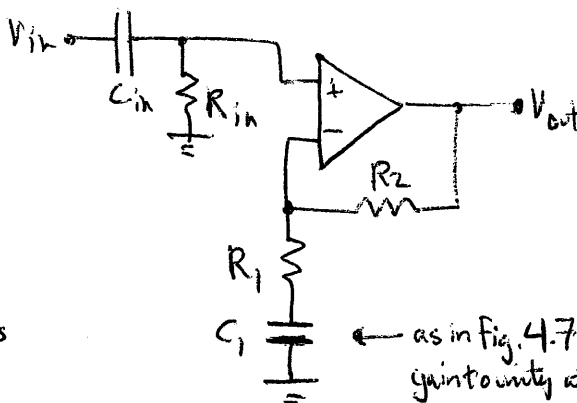
20 dB gain $\Rightarrow A_v = 10$

on p. 178, we find

$A_v = 1 + \frac{R_2}{R_1}$ for this configuration so ...

$\frac{R_2}{R_1} = 9$

... may choose $R_1 = 2.0k$ and $R_2 = 18k$ as in fig. 4.6



To get $Z_{in} = 10k$ in the passband ... choose $R_{in} = 10k$

To get $f_{3dB} = 20Hz$, choose C_{in} such that $\frac{1}{2\pi R_{in} C_{in}} = 20Hz$ or $C_{in} = 0.8 \mu F$

and choose C_1 such that $\frac{1}{2\pi R_1 C_1} = 20Hz$ $C_1 = 4 \mu F$

8.2 (a) Convert 1110101.0110_2 to decimal (base 10).

$$\begin{aligned}
 &= 2_{10}^6 + 2_{10}^5 + 2_{10}^4 + 2_{10}^2 + 2_{10}^0 + 2_{10}^{-2} + 2_{10}^{-3} \\
 &= 64_{10} + 32_{10} + 16_{10} + 4_{10} + 1_{10} + 0.25_{10} + 0.125_{10} \\
 &= \boxed{117.375_{10}}
 \end{aligned}$$

(b) Convert $11.0101\overline{01}_2$ to decimal (base 10)

$$= 2_{10}^1 + 2_{10}^0 + (.0101\overline{01}_2)$$

$$= 3_{10} + \underbrace{.0\overline{1}_2}_{\text{repeating}}$$

let $X = .\overline{01}_2$

then $.0\overline{1}_2 \times 100_2 = 1.\overline{01}_2 = 100_2 X$

$$100_2 X - X = 1_2$$

$$(100_2 - 1_2) X = 1_2$$

$$11_2 X = 1_2$$

$$\text{so } X = \frac{1_2}{11_2} = \frac{1_{10}}{3_{10}} = \left(\frac{1}{3}\right)_{10}$$

Therefore ... $\boxed{11.0\overline{1}_2 = \left(3\frac{1}{3}\right)_{10}}$

(c) Convert $2A_{16}$ to decimal

$$= 2 \times 16_{10}^1 + 10 \times 16_{10}^0 = \boxed{26_{10}}$$

(d) Convert 1023_{10} to binary...

note that $1024_{10} = 2^{10}$ so ... $1023_{10} = 2_{10}^{10} - 1$

$$= 100000000000 - 1 = \boxed{1111111111_2}$$

(e) Convert 1023_H to binary.

Easier (for me) to first convert to decimal ...

$$1 \times 16_{10}^3 + 2 \times 16_{10}^1 + 3 \times 16_{10}^0 = 4096_{10} + 32 + 3 = \underline{\underline{4131_{10}}}$$

Use method on p.474.

$$\frac{4131}{2} = 2065 \quad \text{remainder } 1$$

$$\frac{2065}{2} = 1032 \quad \text{remainder } 1$$

$$\frac{1032}{2} = 516 \quad \text{remainder } 0$$

$$\frac{516}{2} = 258 \quad \text{remainder } 0$$

$$\frac{258}{2} = 129 \quad \text{remainder } 0$$

$$\frac{129}{2} = 64 \quad \text{remainder } 1$$

$$\frac{64}{2} = 32 \quad \text{remainder } 0$$

$$\frac{32}{2} = 16 \quad \text{remainder } 0$$

$$\frac{16}{2} = 8 \quad \text{remainder } 0$$

$$\frac{8}{2} = 4 \quad \text{remainder } 0$$

$$\frac{4}{2} = 2 \quad \text{remainder } 0$$

$$\frac{2}{2} = 1 \quad \text{remainder } 0$$

$$\frac{1}{2} = 0 \quad \text{remainder } 1$$

so. $1023_H = 4131_{10} = 1000000100011_2$

(f) Convert 1023_{10} to hexadecimal

By the same method as above...

$$\frac{1023}{16} = 63 \text{ remainder } 15 \text{ (F)}$$

$$\frac{63}{16} = 3 \text{ remainder } 15 \text{ (F)}$$

$$\frac{3}{16} = 0 \text{ remainder } 3 \text{ (3)}$$

so... $1023_{10} = 3FF_H$

(g) Convert 101110101101_2 to hexadecimal

First convert to decimal...

$$101110101101_2$$

$$= \cancel{2^{10}} + \cancel{2^9} + \cancel{2^8} + \cancel{2^7} + \cancel{2^6} + \cancel{2^4} + \cancel{2^2} + 2^1$$

$$= 2^{11} + 2^9 + 2^8 + 2^7 + 2^5 + 2^3 + 2^2 + 2^0$$

$$= 2048 + 512 + 256 + 128 + 32 + 8 + 4 + 1 = 2989_{10}$$

$$\frac{2989}{16} = 186 \text{ remainder } 13 \text{ (D)}$$

$$\frac{186}{16} = 11 \text{ remainder } 10 \text{ (A)}$$

$$\frac{11}{16} = 0 \text{ remainder } 11 \text{ (B)}$$

$101110101101_2 = 2989_{10} = BAD_H$

(b) Convert 61453_{10} to hexadecimal

$$\frac{61453}{16} = 3840 \quad \text{remainder } 13 \quad (D)$$

$$\frac{3840}{16} = 240 \quad \text{remainder } 0 \quad (0)$$

$$\frac{240}{16} = 15 \quad \text{remainder } 0 \quad (0)$$

$$\frac{15}{16} = 0 \quad \text{remainder } 15 \quad (F)$$

$61453_{10} = F00D_H$

8.5 Use an exclusive-OR gate as an optional inverter



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Use B as the control ... if $B=0$ then...

A	Q
0	0
1	1

and the gate acts as a buffer without inversion

if $B=1$ then

A	Q
0	1
1	0

and the gate acts as an inverter.

8.7

What do the circuits in Fig. 8.12 do?

A:



NOR gate Truth Table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

A	Q
0	1
1	0

This is an inverter!

B:



AND Truth Table

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

A	Q
0	0
1	1

This is a buffer!

C:



NOR

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

A	Q
0	1
1	0

This is also an inverter!

D:



NOR

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

B	Q
0	0
1	0

Always returns a Low output.

E:



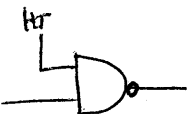
AND

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

A	Q
0	0
1	0

Always returns a Low output.

F:



NAND

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

B	Q
0	1
1	0

This is an inverter,

8.8

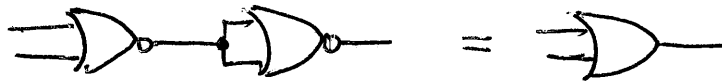
Using 2-input gates show how to ~~use~~ make

(a) INVERT from NOR ... see 8.7 part A or part C



(b) OR from NORs ...

OR = NOT NOR so ...



(c) OR from NANDs ...

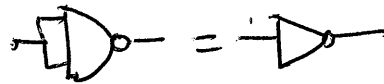
NAND $\Rightarrow \overline{A \cdot B} = \bar{A} + \bar{B}$ by DeMorgan's Theorem

or starting with $A + B = \overline{\overline{A + B}} = \overline{\bar{A} \cdot \bar{B}}$

A OR B = NOT (NOT A and NOT B)
 NAND (NOT A, NOT B)

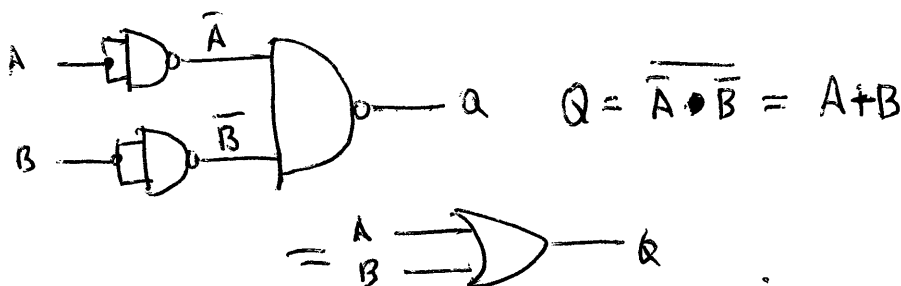


Note that a NAND gate with both inputs connected together is an inverter



NAND		Q
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

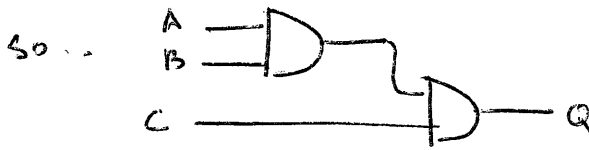
so ...



8.9

(a) Make a 3-input AND gate from 2-input ANDs...

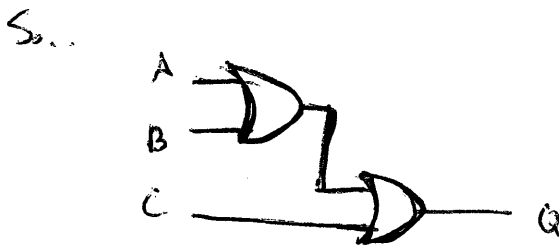
Note that $A \cdot B \cdot C = (A \cdot B) \cdot C = A \cdot (B \cdot C)$
(see p. 491, table 8.3)



A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(b) Make a 3-input OR gate from 2-input ORs

Note that $A + B + C = (A + B) + C = A + (B + C)$
(see p. 491, table 8.3)



A	B	C	Q
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(c) Make a 3-input AND from 2-input NANDs

Since we can make INVERTERS out of NANDs...

