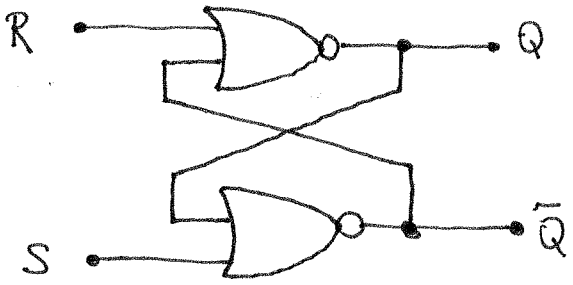
Notes on Flip-flops ... the basic unit of digital electronic memory

- Consider the cross-coupled NOR gates ...



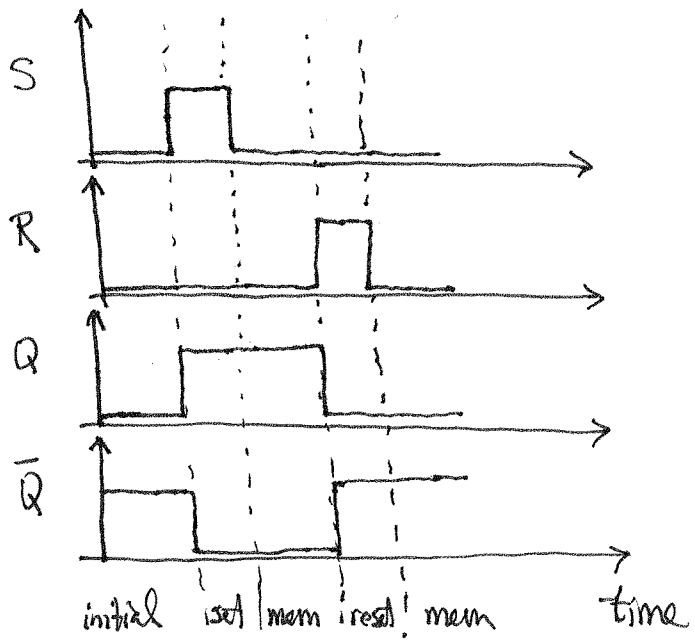
NOR Truth table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

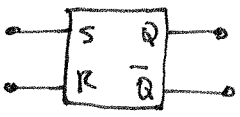
Truth table for this RS Flip-flop

S	R	Q	$\bar{Q}$	
0	0	{1	0}	memory state ... stores last HI input as Q
		0	1	
0	1	0	1	"reset"
1	0	1	0	"set"
1	1	0	0	undesirable state ... avoid this combination of inputs

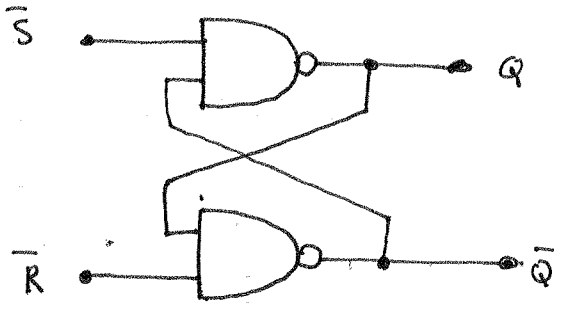
Time sequence of inputs



Circuit symbol for RS flip-flop



- Another version of the RS flip-flop using NAND gates.



↑ bar indicates "active low" inputs

That is... "set" the flip-flop by making $\bar{S}$ low

"reset" " " " $\bar{R}$ low

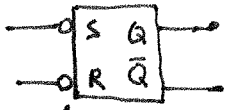
NAND Truth Table

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

Truth table

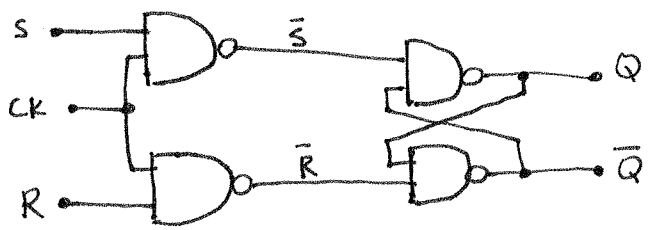
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
0	0	1	1	undesirable state
0	1	1	0	"set"
1	0	0	1	"reset"
1	1	1	0	memory state... stores last LO input as Q
		0	1	

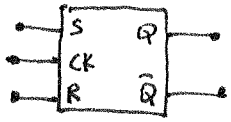
Symbol



↑ active-low inputs

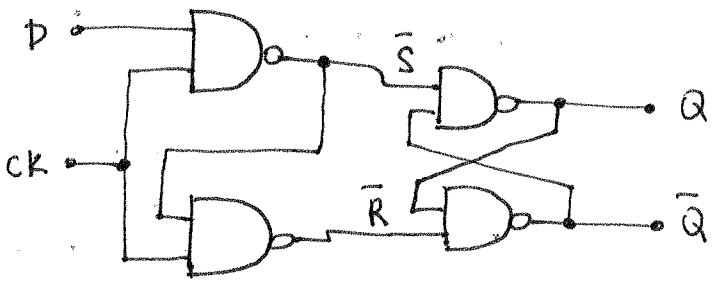
- Clocked Flip-flop





CK	S	R	$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
0	0	1	1	1	1	0	"latched" or memory state
	1	0			0	1	
1	0	0	1	1	1	0	"latched" or memory state
					0	1	
1	0	1	1	0	0	1	reset
1	1	0	0	1	1	0	set
1	1	1	0	0	1	1	undesirable state

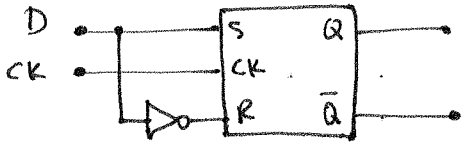
- The D flip-flop or "data latch"



CK	D	$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
0	1	1	1	1	0	latched/memory
	0			0	1	
1	0	1	0	0	1	reset
1	1	0	1	1	0	set

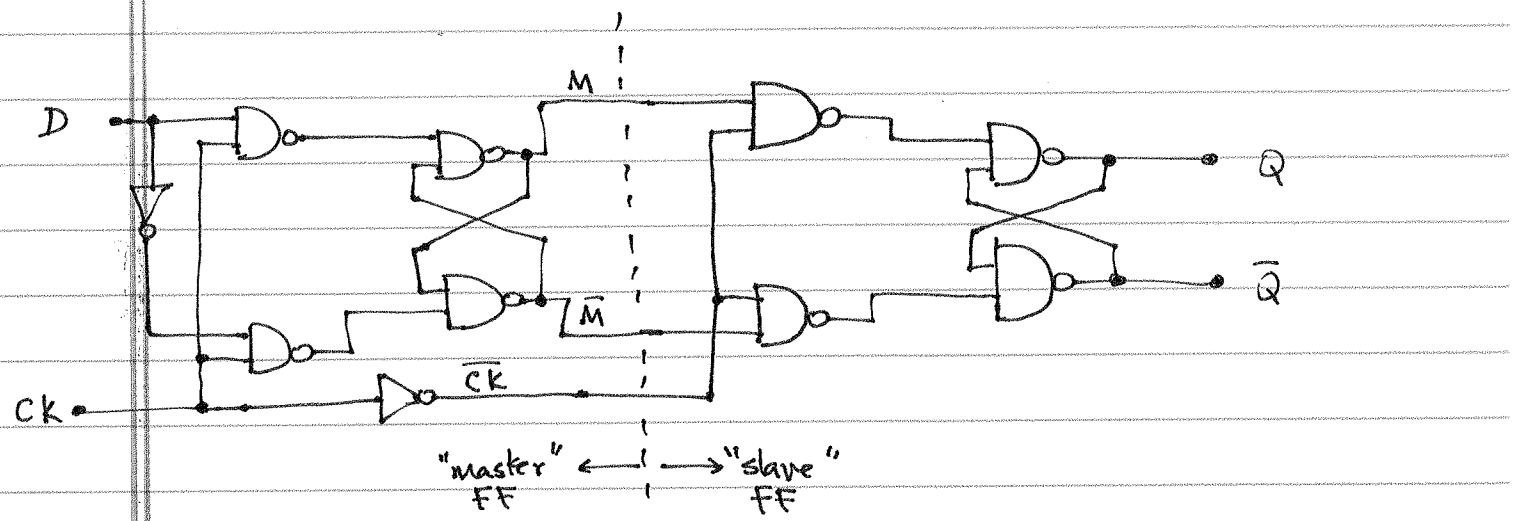
no undesirable state!

- Can make a D flip-flop using a RS flip flop and an inverter.



S and R are always complementary so the output Q will be the state of the D input when the CK was last HI.

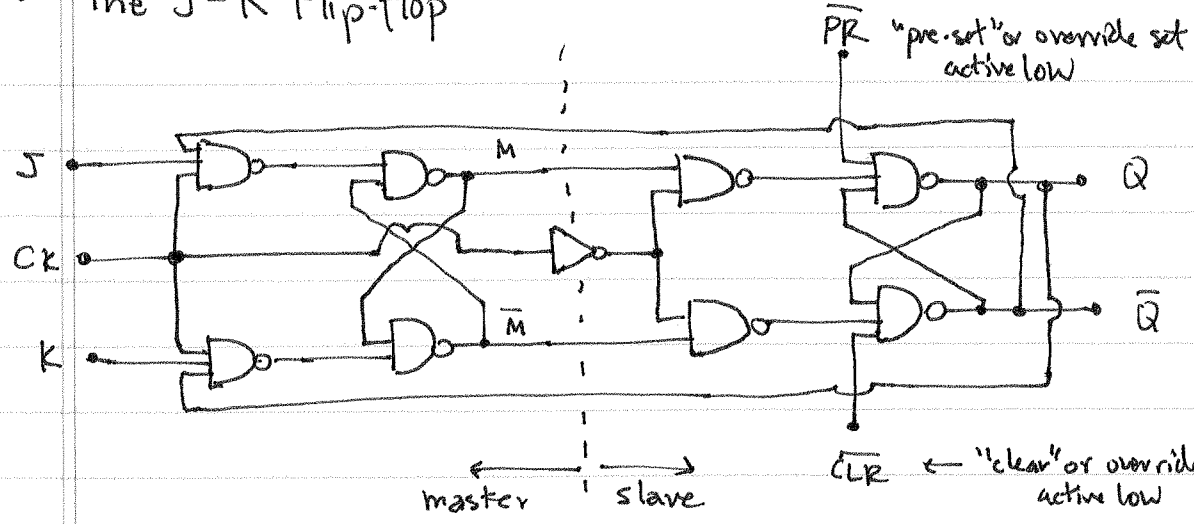
- A "Master-slave" Flip-flop
  ↑ unfortunately this is the standard terminology

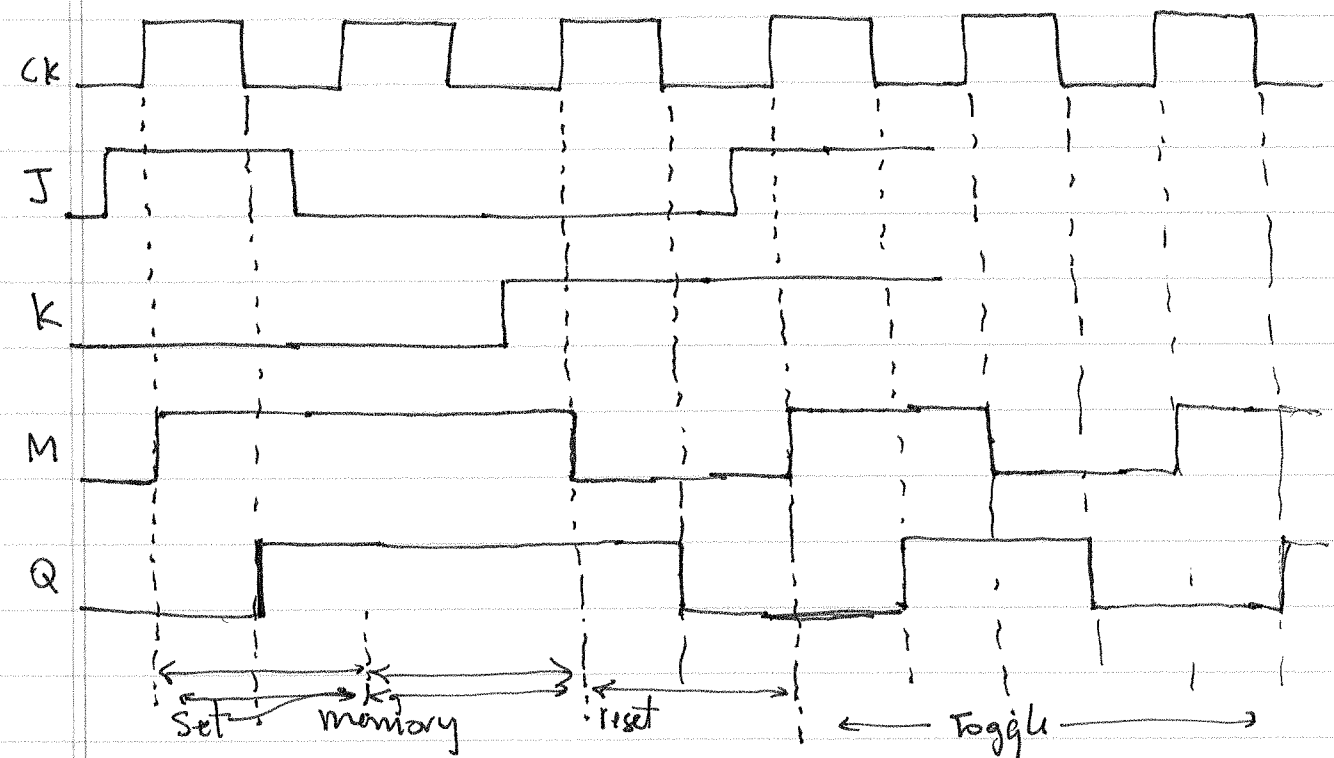


When CK is HI, the master FF is "enabled", passing D to the M output (and $\bar{M} = \bar{D}$).
During this time the slave FF is "disabled" since its $\overline{CK}$ input is LO so Q and $\bar{Q}$ hold onto whatever state they had when $\overline{CK}$ was last HI

When CK is LO, the master FF is disabled, and the slave FF is enabled. The M/$\bar{M}$ inputs are then passed to the output $Q = M$, $\bar{Q} = \bar{M}$.

- The J-K Flip-flop



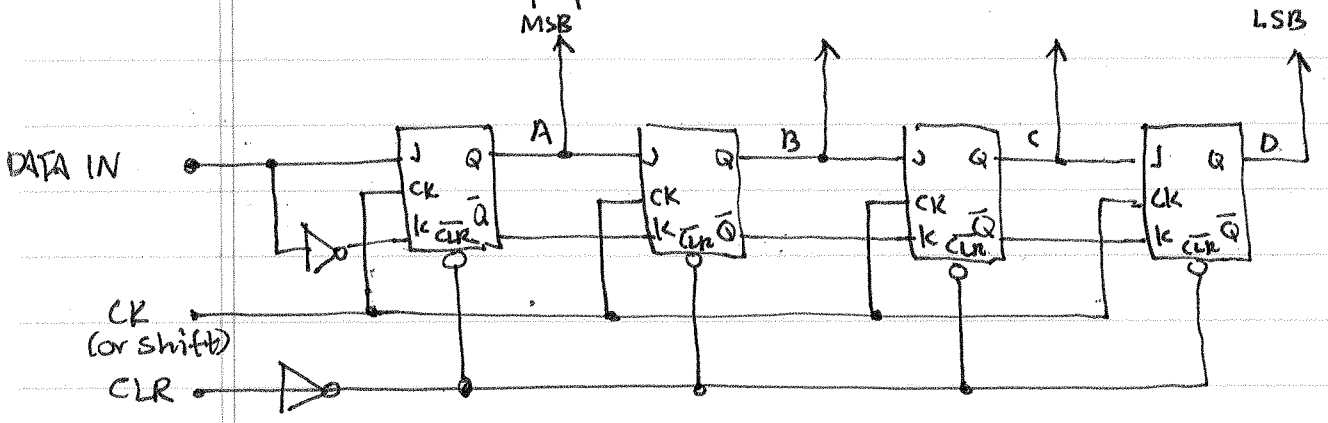


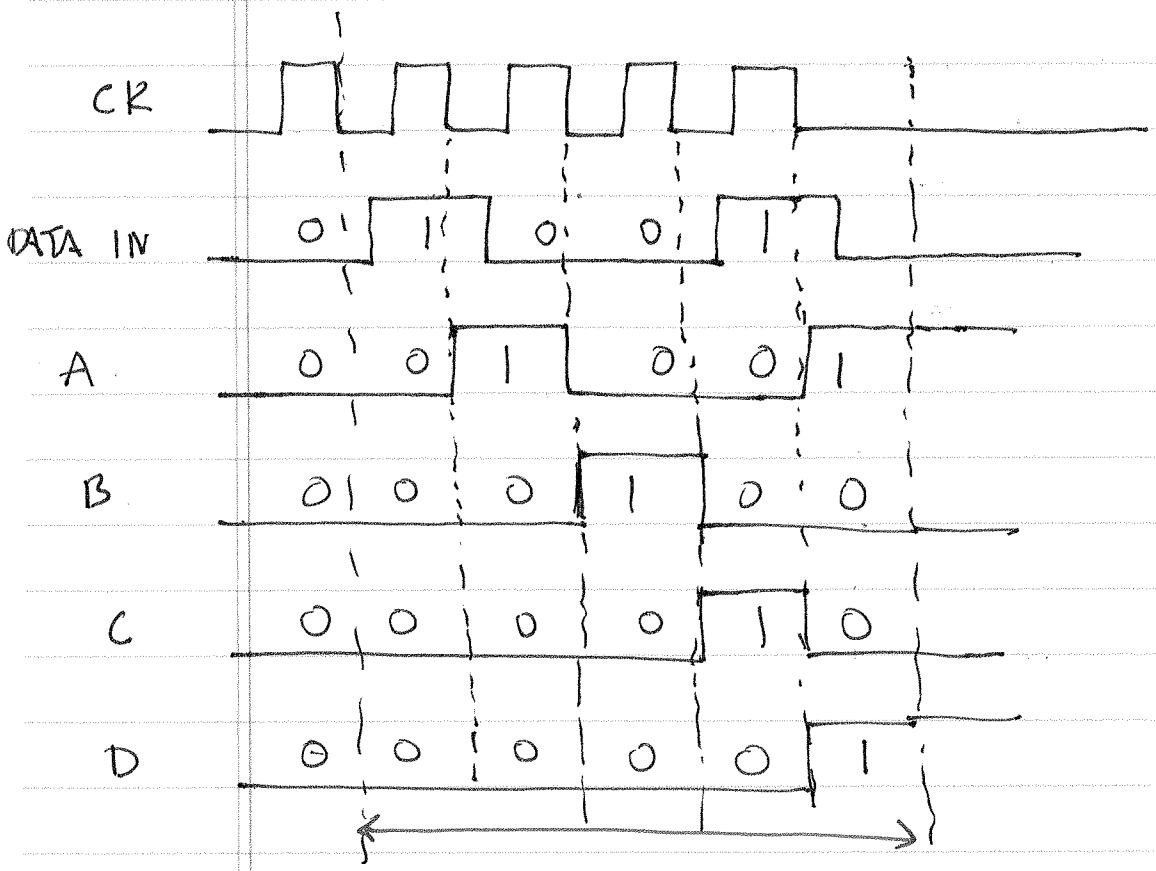
Truth table — on rising edge of CK → on falling edge of CK

J	K	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	Q_n	$\overline{Q}_n$	memory
0	1	0	1	reset
1	0	1	0	set
1	1	$\overline{Q}_n$	Q_n	toggle

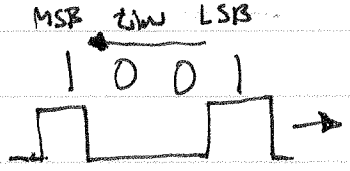
A Shift Register

Serial to papallel data conversion





4 bit word read into the shift register



A 1
B 0
C 0
D 1

Should do example that is not time reversible

• One-shots or Monostable Multivibrators or Pulse Stretchers