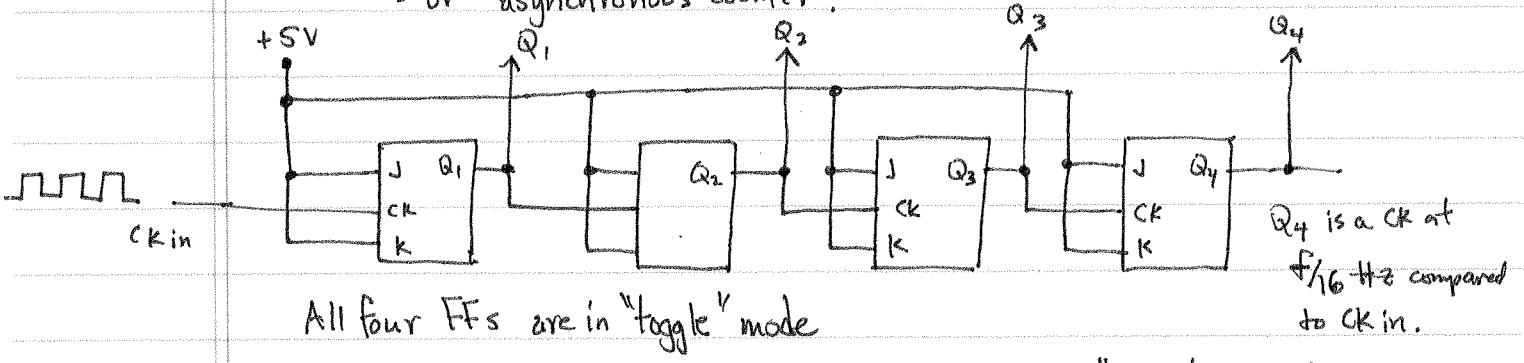
PHYS 220 Physical Electronics Fall 2010

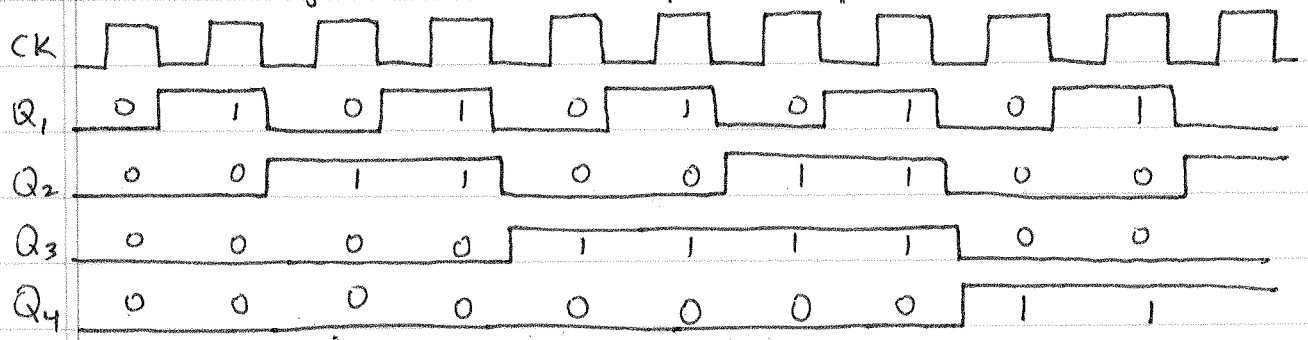
Notes on Digital Counters

- Four bit "ripple counter" uses 4 JK Flip-flops
  ↕ or "asynchronous" counter.



All four FFs are in "toggle" mode

Timing diagram ... the changes in the output 4-bit number "ripple" through the register due to the finite response time of the flip-flops.

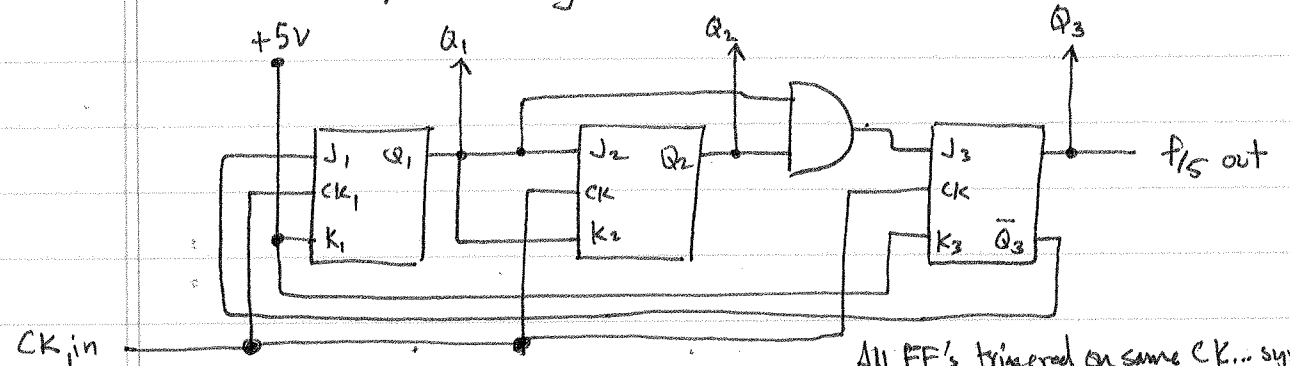


Read output states with Q_4 as MSB and Q_1 as LSB...

CK pulse	Q_4	Q_3	Q_2	Q_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	0	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

↓ Binary counting from 0 to 15. before repeating

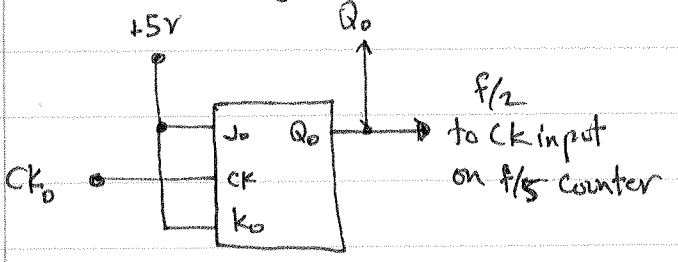
• A Divide-by-five Synchronous Counter



All FF's triggered on same CK... synchronous

CK pulse	J_1	K_1	FF_1 state	J_2	K_2	FF_2 state	J_3	K_3	FF_3 state	Q_3	Q_2	Q_1	binary count
0	1	1	T	0	0	M	0	1	R	0	0	0	from 0 to 4
1	1	1	T	1	1	T	0	1	R	0	0	1	
2	1	1	T	0	0	M	0	1	R	0	1	0	
3	1	1	T	1	1	T	1	1	T	0	1	1	
4	0	1	R	0	0	M	0	1	R	1	0	0	
5	1	1	T	0	0	M	0	1	R	0	0	0	repeat

To get a nearly synchronous binary counter from 0 to 9 (÷ by 10 counter)
add a divide by 2 to the front-end driving the CK input to the ÷5 counter above.



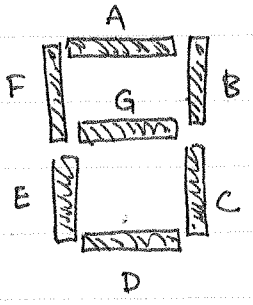
This FF will toggle every CK cycle... giving the f/5 counter
a clock that is f/2 ...

CK_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1
1	0	0	1	0
2	0	0	1	1
3	0	1	0	0

etc...

When output gets to 1001, it will repeat
... 0 to 9 counter !!

- Seven-segment LED display



Each segment is a light-emitting diode

emits light when forward-biased ... conducting.

Anodes are held HI. Segment lights up when cathode is LO

Decimal (CK$_0$)	Binary-Coded Decimal (÷10) Counter				7-segment display cathode state.							Display
	Q_3	Q_2	Q_1	Q_0	A	B	C	D	E	F	G	
0	0	0	0	0	0	0	0	0	0	0	1	
1	0	0	0	1	1	0	0	1	1	1	1	
2	0	0	1	0	0	0	1	0	0	1	0	
3	0	0	1	1	0	0	0	0	1	1	0	
4	0	1	0	0	1	0	0	1	1	0	0	
5	0	1	0	1	0	1	0	0	1	0	0	
6	0	1	1	0	1	1	0	0	0	0	0	
7	0	1	1	1	0	0	0	1	1	1	1	
8	1	0	0	0	0	0	0	0	0	0	0	
9	1	0	0	1	0	0	0	1	1	0	0	

BCD-to-7segment decoder

logic gates!!